AMENDMENTS TO THE DRAWINGS:

The attached replacement sheet of drawings include changes to FIG. 1. Reference numerals have been added to FIG. 1 in order to provide additional clarification in accordance to the originally filed specification. No new matter has been added.

REMARKS

The Office Action of June 27, 2007 was received and carefully reviewed. Reconsideration and withdrawal of the currently pending rejections are requested for the reasons advanced in detail below.

Claims 1-11 were pending prior to the instant amendment. By this amendment, claims 12-15 are added. Consequently, claims 1-15 are currently pending in the instant application.

Claims 10 and 11 were rejected under 35 U.S.C. §103(a) as being anticipated over Wataru et al. (JP 2003-046490) in view of Hideki et al. (JP 2002-165148). Wataru et al. and Hideki et al., however, fail to render the claimed invention unpatentable. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. For example, independent claim 10 recites a combination that includes, among other things:

> a packet deletion circuit provided on the input side of the FIFO . . . a packet addition circuit provided on the output side of the FIFO,

At the very least, Wataru et al. and Hideki et al. fail to disclose or suggest any of these exemplary features recited in independent claim 10.

The Examiner has failed to establish a *prima facie* case of obviousness for at least four reasons. First, the Examiner has not demonstrated how Wataru et al. and Hideki et al., whether taken alone or in combination, disclose or suggest each and every feature recited in the claims. *See* M.P.E.P. § 2143 (7th ed. 1998). Second, the Examiner has not shown the existence of any reasonable probability of success in modifying Wataru et al., the base reference, based on the teachings of Hideki et al., the secondary reference, in a manner that could somehow result in the claimed invention. *See id.* Third, the Examiner has not

identified any suggestion or motivation, either in the teachings of the applied references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the apparatus of Wataru et al. in a manner that could somehow result in the claimed invention. *See id.* Finally, the Examiner has not explained how his obviousness rationale could be found in the prior art — rather than being a hindsight reconstruction of Applicants' own disclosure. *See id.*

Each of the Examiner's factual conclusions must be supported by "substantial evidence" in the documentary record, as required by the Federal Circuit. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1435 (Fed. Cir. 2002). The Examiner has the burden of documenting all findings of fact necessary to support a conclusion of anticipation or obviousness "less the 'haze of so-called expertise' acquire insulation from accountability." *Id.* To satisfy this burden, the Examiner must specifically identify where support is found within the prior art to meet the requirements of 35 U.S.C. §§ 102(b) and 103. In this case, however, the Examiner has failed to satisfy his burden of demonstrating how Wataru et al., taken alone or in combination with Hideki et al., can either anticipate or render obvious each and every one of the limitations present in independent claim 10, as required by the MPEP and Federal Circuit jurisprudence.

The present invention provides a control device having a packet deletion circuit and packet addition circuit. The packet deletion circuit is provided on the input side of a jitter buffer (FIFO) corresponding to a result of monitoring a stored packet quantity in the jitter buffer. Thus, the invention is able to prevent deleting packets which were stored in the jitter buffer.

Additionally, a packet addition circuit is provided on the output side of the jitter buffer corresponding to a result of monitoring. Thus, the invention is able to prevent

becoming distorted when reproducing sound by adding an additional packet to an outputted packet which is to be further decoded as data from the jitter buffer.

Turning to the cited prior art, Wataru et al. is concerned with providing a voice transmission device capable of realizing a clock difference absorbing function with higher voice quality and high precision at a low cost, which can absorb a difference of clock signals between a transmitter side device and a receiver side device. The Examiner states (see, e.g., Office Action at paragraph 7) that Wataru et al. discloses "a packet de[t]ection circuit provided on the input of the FIFO," and references Wataru et al. at paragraph 33, line 12. In addition, the Examiner states that Wataru et al. discloses "a packet addition circuit provided on the output side of the FIFO," and references Wataru et al. at paragraph 33, line 7.

However, upon review of Wataru et al. at the reference locations given by the Examiner, a teaching of the structure of the present invention is found lacking as recited by Applicants' claims. At best, Wataru et al. discusses inserting a non-note numberized sound signal directed in the non-note numberized sound signal generation section 13. The reference also discusses discarding a non-note numberized sound signal of the silent section by the first-sound voice frame which is performed in step S5. The corresponding figures of FIGS. 1 and 2, further, fail to disclose for fairly suggest the embodiments of the claimed structure. For example, the packet deletion circuit provided on the input side the FIFO is not disclosed by Wataru et al. as recited in the present claims. Furthermore, the packet addition circuit provided on the output side of the FIFO is also not disclosed by Wataru et al. as recited in the present claims. The Examiner attempts to remedy the deficiencies Wataru et al. by turning to the teachings of Hideki et al. However, Hideki et al. fails to cure the deficiencies of Wataru et al., because it also lacks a disclosure of the structure as recited in Applicants' claims.

In accordance with the M.P.E.P. § 2143.03, to establish a *prima facie* case of obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 409 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 196 (CCPA 1970). Therefore, it is respectfully submitted that neither Wataru et al. or Hideki et al., taken alone or in any proper combination, discloses or suggests the subject matter as recited in claim 10. Hence, withdrawal of the rejection is respectfully requested.

Each of the dependent claims depend from independent claim 10 and are patentable over the cited prior art for at least the same reasons as set forth above with respect to claim 10.

In addition, each of the dependent claims also recite combinations that are separately patentable.

In view of the foregoing remarks, this claimed invention, as amended, is not rendered obvious in view of the prior art references cited against this application. Applicant therefore request the entry of this response, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

In discussing the specification, claims, and drawings in this response, it is to be understood that Applicant in no way intends to limit the scope of the claims to any exemplary embodiments described in the specification and/or shown in the drawings. Rather, Applicant is entitled to have the claims interpreted broadly, to the maximum extent permitted by statue, regulation, and applicable case law.

Should the Examiner believe that a telephone conference would expedite issuance of the application, the Examiner is respectfully invited to telephone the undersigned patent agent at (202) 585-8316.

Respectfully submitted,

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